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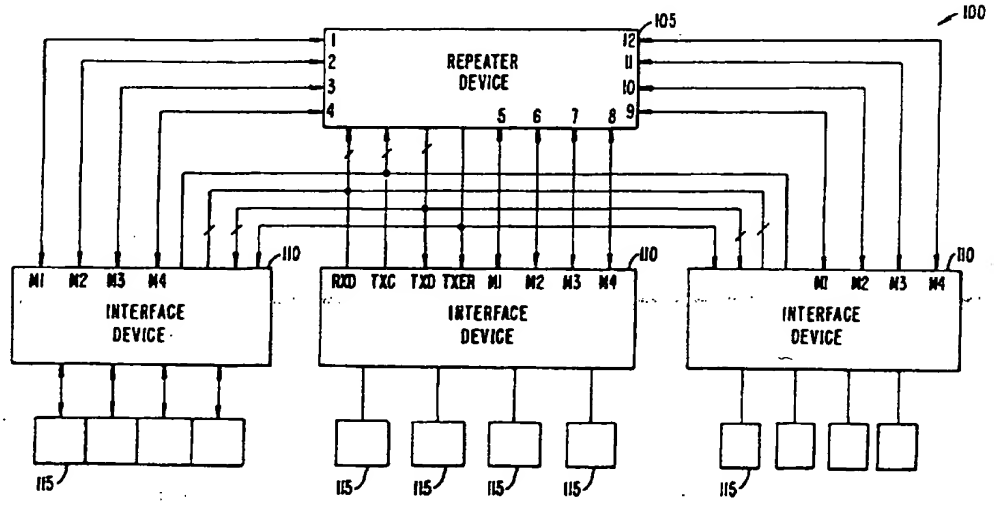

(57) Abstract

A media independent interface for interconnecting an integrated repeater front-end with one or more integrated interface devices, each having several physical layer devices for operation in conformance with IEEE 802.3u. The media independent interface, in a repeater implementation, shares transmit and receive data channels, and provides for dedicated control signals, thereby multiplexing shared channels across all of the physical layer devices in the integrated interface device.

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OPTIMIZED MII FOR 802.3u (100 BASE-T) FAST ETHERNET PHYs

BACKGROUND OF THE INVENTION

The present invention relates generally to interconnecting PHY devices in a computer local area network, and more specifically to an optimized interface between an integrated repeater front-end and an integrated interface device having multiple PHY devices in such a network.

Computer networks are commonly used in today's business environment. One common network structure uses one or more repeaters in a star topology, each repeater having several ports. A particular data packet received at one port is retransmitted to all other ports of the repeater. Each repeater restores timing and amplitude degradation of data packets received on one port and retransmits them to all other ports, and hence over the entire network. In networks employing CSMA/CD, such as an Ethernet network, every data packet passes through every repeater.

Traditional Ethernet networks (10BASE-T) operate at 10Mb/s. A standard promulgated by the IEEE (IEEE Standard 802.3), hereby incorporated by reference for all purposes, defines various functionality for such computer networks. Modernly, Ethernet networks are being upgraded to support 100Mb/s operation. Standard IEEE 802.3u, hereby incorporated by reference for all purposes, defines the functionality for such high speed networks. The Standard defines operation of 100BASE-T systems using unshielded twisted pair (UTP) physical media types. For 100BASE-TX, the specification defines operation over 2 pairs of category 5 (CAT 5) UTP. For 100BASE-T4, the specification defines operation over 4 pairs of Cat 3 UTP. Additionally, 802.3u includes a 100BASE-FX specification that allows operation over dual fiber optic cabling.

The physical layer interface (PHY) defines the physical signaling scheme between two communicating devices. Many networks often use many PHY devices operating over

different media types. In order to allow data terminal equipment (DTE) or a repeater to use whichever medium is more suitable, the PHY in 100BASE-T is segregated by a Media Independent Interface (MII), which is essentially analogous to the AUI of 10Mb/s Ethernet. In 10Mb/s Ethernet, the AUI is an interface consisting of only six "channels", but in 100Mb/s operation, the interface is increased to eighteen signal "channels" in the MII. When integrated into a semiconductor device or package such as a physical housing, the channels are embodied as physical pins on the interface.

In 10BASE-T operating at 10Mb/s, the Ethernet/802.3 repeaters have become extremely integrated. As Ethernet has been upgraded to support 100Mb/s operation, it has become more difficult to implement a cheap, single chip, low pin count package which houses the entire repeater functionality, especially if multiple PHY devices are integrated together.

In 100BASE-T operation, a repeater is ideally constructed to allow some or all of its ports to be connected to any MII based PHY device. However, given the eighteen pin overhead per MII, production of integrated repeater solutions becomes more costly. A repeater front-end chip which has all MII ports for multiple PHY devices would almost certainly make the chip "pad limited". In conventional silicon processing technologies, this means that there will be so many pads for interconnect to the external device pins, that the spacing of the pads will determine the die size of the chip. Furthermore, there will be inadequate additional complexity in the logic of the chip to fill the available silicon real estate enclosed by the pad ring. Larger, more expensive chips will have to be produced to accommodate the higher pin count package which houses the entire repeater functionality. Clearly, it is desirable to reduce the pin overhead in a repeater chip, while still allowing the repeater front-end chip to connect and operate with any MII based PHY device.

SUMMARY OF THE INVENTION

The present invention provides a device for economically and efficiently interfacing a plurality of PHY devices integrated into a single semiconductor package (interface device) with an integrated repeater front-end device to produce a repeater. Making effective use of the available pins and by use of innovative design of the features of multiple integrated PHY devices, the preferred embodiment permits an effective solution that is more cost-effective than a prior art solution of simply adding additional pins. As the number of PHY devices integrated into a single package increases, the preferred embodiment of the present invention increasingly saves pin count and attendant reliability.

In the course of integrating the multiple PHY devices, a preferred embodiment of the present invention provides for an integrated device capable of having a flexibility to interoperate with any of the 100BASE-T media types in addition to enhanced functionality. Some of these features include the ability to control transmission of security symbols for security (eavesdrop protection) using a standard MII, integration of a Carrier Integrity Monitor (CIM) state machine into the interface device to improve backward compatibility with repeater front-ends that do not implement the CIM, programmable mode control to reconfigure certain channels depending upon the environment or operational specifications. One aspect of the preferred embodiment addresses steering input ports to appropriate repeaters, such as for speed matching, load balancing or port mobility, for example. It is possible to create a dual speed repeater for 10Mb/s and 100Mb/s operation.

According to one aspect of the invention, it includes a first and a second PHY device for coupling to a repeater front-end. The PHY devices communicate with the repeater front-end by use of a multiplexed MII, wherein receive and transmit data channels are shared by the PHY devices and some control channels are dedicated to each PHY device.

According to another aspect of the invention, it includes a first and a second PHY for coupling to a repeater front-end, each PHY having a media independent interface. The PHY devices communicate with the repeater front-end in two different modes of operation. In one mode the PHY acts normally, while in the second mode the transmit error and receive error channels are reconfigured to operate as additional transmit and receive channels, respectively.

In yet another aspect, it includes a first PHY for coupling to a first repeater and a second PHY for coupling to a second repeater. A switch connected to both PHYs allows incoming data to one of the first and second PHYs be switched to either the first repeater of the second repeater.

A further aspect includes a PHY having a media independent interface for coupling to a repeater front-end, that operates in two modes. In one mode the collision channel operates as normal. In the second mode the collision channel is configured as a false carrier channel.

Yet a further aspect includes a security device for use with a repeater, wherein a PHY is connected to a repeater front-end. The repeater transmits a security signal to the PHY using dedicated transmit error and transmit enable channels. The PHY then responds to the received security signal by outputting a security symbol.

Another aspect includes a PHY having transmit, receive and control channels for connecting to a repeater front-end. The PHY also includes a carrier integrity monitor (CIM) for monitoring activity on the input channels of the PHY, wherein the CIM can be selectively enabled or disabled.

Reference to the remaining portions of the specification, including the drawing and claims, will realize other features and advantages of the present invention. Further features and advantages of the present invention, as well as the structure and operation of various embodiments of the present invention, are described in detail below with respect to accompanying drawing. In the drawing, like reference numbers indicate identical or functionally similar elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic block diagram of a repeater including an integrated repeater front-end device and a group of interface devices including, in the preferred embodiment, a plurality of fast Ethernet transceivers that conform to the incorporated 802.3u IEEE standard;

Fig. 2 is a schematic plan view of the integrated interface device shown in Fig. 1;

Fig. 3 is a schematic plan view of an alternate pin out option of an integrated switch interface device using the same internal semiconductor device packaged for the integrated interface device shown in Fig. 2; and

Fig. 4 is a schematic diagram of a dual repeater including a first repeater device, a second repeater device, a network device to interconnect the first repeater device with the second repeater device, two switches and two switch interface devices (first switch interface device and second switch interface device).

DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a schematic block diagram of a repeater 100 including an integrated repeater front-end device 105 and a group of integrated interface devices 110 including, in the preferred embodiment, a plurality of Fast Ethernet transceivers that conform to the incorporated 802.3u IEEE standard. Each interface device 110 services a number of ports, each port coupled in turn to a network device 115, which may be a repeater, for example. In the preferred embodiment, each interface device 110 includes four physical layer (PHY) devices (not shown), one PHY per port, and repeater device 105 is coupled to three interface devices 110 to provide repeater 100 with a total of twelve ports.

The repeater device 105 and each interface device 110 are separately integrated into individual semiconductor devices that are interconnected to form repeater 100. Some applications will have different configurations for the number of interface devices 110 per repeater device 105 and/or different number of PHY devices per interface device 110,

dependent upon design and cost consideration goals.

In the preferred embodiment, each integrated PHY conforms to the IEEE 802.3u standard, except as set forth below when implementing enhanced functionality. Each PHY device communicates with repeater device 105 by use of a modified media independent interface (MII) as further described by reference to Fig. 2.

Fig. 2 is a schematic plan view of integrated interface device 110. The interface device 110 includes four dedicated signal ports, each marked as MII 200. Each MII 200 includes a receive clock (RXC) channel, a receive data valid (RX_DV) channel, a collision (COL) channel, a carrier sense (CRS) channel, a receive error (RX_ER) channel and a transmit enable (TX_EN) channel for a total of six channels per dedicated signal port. These six channels are port specific channels dedicated to each PHY device of integrated interface device 110.

In addition, to complete the modified MII, each PHY device shares twelve common channels into repeater device 105. Two of the shared common channels are a management data clock (MDC) channel and a management data input/output (MDIO) channel. Further, four receive data (RXD<3:0>) channels, four transmit data (TXD<3:0>) channels, a transmit clock (TXC) channel and a transmit error (TX_ER) channel. Table I, below, further explains the function of the MII channels. Hence, each PHY device uses its dedicated port channels as well as the shared channels to communicate with the repeater device 105.

TABLE I

TXD <3-0>	Transmit Data. 4 pins for transmit data sent by the repeater or DTE to be transmitted by the PHY on the medium.
RXD <3-0>	Receive Data. 4 pins for received data recovered by the PHY from the medium and passed to the repeater or DTE.
RXC	Receive Clock. The clock decoded by the PHY from the incoming data from the medium.
TXC	Transmit Clock. The PHY's own clock, passed to the DTE or repeater, and used to clock data from the repeater/DTE.
TX_ER	Transmit Error. A signal asserted by the repeater (or optionally DTE) to indicate to the PHY(s) that a coding violation was detected in the received signal stream.
RX_ER	A signal from the PHY to indicate to the repeater or DTE that a coding violation was detected in the PHY's received data.
TX_EN	Transmit Enable. Asserted by the repeater or DTE to indicate that valid data is being presented on the TXD pins.
RX_DV	Receive Data Valid. Asserted by the PHY to indicate to the repeater or DTE that valid data is being presented on the RXD pins.
CRS	Carrier Sense. Asserted by the PHY to indicate receive medium activity.
COL	Collision. Asserted by the PHY to indicate that a collision condition has been detected on the medium.
MDIO	Management Data Input Output. A bi-direction line that allows serial data to be clocked in and out of the PHY device.
MDC	Management Data Clock. The clock signal used for synchronously transferring data in and out of the PHY using the MDIO pin.

In operation, data from only one receive port is decoded at any time. Simultaneous activation of receive activity on two or more ports constitutes a collision. Thus, repeater device 105 does not require the actual data from more than one receive port at any time. Detection of two simultaneous receive functions causes repeater device 105 to

initiate transmission of jam signals from all the ports.

Repeater device 105 determines which port to associate with received data on the shared data channels by use of the dedicated RX_DV and CRS channels associated with the receiving port. Only one PHY device, the one receiving data, asserts its RX_DV and CRS channels. The repeater device 105 reads the shared RXD channels synchronized by the RXC channel.

Repeater device 105 retransmits the received data to all other active and enabled ports. Repeater device 105 asserts the received data on the shared transmit channels and asserts TX_EN to all active and enabled PHY ports, except the receiving PHY device. The received data is transmitted from each transmitting PHY device synchronized with the TXC channel.

During the receipt and transmission of data, any collision detected by the receiving PHY device is communicated to the repeater device 105, such as by asserting the COL channel. Additionally, any other PHY device asserting RX_DV to repeater device 105 while another PHY device is receiving data signals a collision condition to the repeater device 105.

Receipt of RX_ER at repeater device 105 transmitted from a receiving PHY device causes repeater device 105 to assert TX_ER to all transmitting PHY devices. All transmitting PHY devices thereafter ensure that a code violation symbol occurs in the retransmitted signal.

In the worst case, integrated repeater device 105 would require two hundred sixteen pins (18 pins/port x 12 ports) just to satisfy the channel requirements for three interface devices 110, each having four PHY devices, when a full MII is implemented for each port or PHY device. In the preferred embodiment, a conservative savings is realized because only eighty-two channels ((6 dedicated channels/port x 12 ports) + 10 shared channels) are needed for three interface devices 110 each having four PHY devices to communicate with repeater device 105, rather than the worst case two hundred sixteen channels.

In some applications, a more aggressive implementation may be used to realize even greater savings on pin count. Sometimes it may be possible to implement RXC as a single channel shared among all PHY devices, or less favorably, shared among all PHY devices of a single interface device 110. The degree to which the various ports may share a common RXC depends upon the degree to which the various ports are synchronized. Completely unsynchronized ports most likely require the configuration of the preferred embodiment (i.e., a dedicated RXC per PHY device). In other applications, it is possible to put some delay budget into the interface device 110, to allow received symbols to be realigned to a single master receive clock (the single shared RXC for all PHY devices).

In some cases, it may be desirable to multiplex only TXD and RXD channels and otherwise have dedicated MII channels. Such an application would be useful to reduce a pin count for a device such as a media access controller (MAC) directly coupled to a repeater device (such as for management). In this way, since the MAC and repeater front-end communicate using half-duplex data exchanges, the total pin complement is reduced but the MAC retains the ability to operate and examine all packet traffic that passes through the repeater device.

Another feature of interface device 110 to provide enhanced functionality is the addition of a disable encoding/decoding (DISENDEC) pin. Interface device 110 includes a four-bit/five-bit encoder/decoder function in each PHY device. In this application, five-bit symbols from the medium are converted to four-bit symbols for use across the MII. Disabling the encoding/decoding by asserting DISENDEC results in using native five-bit symbols across the MII. To obtain the extra channels for the MII without adding pins, assertion of DISENDEC reconfigures TX_ER and RX_ER channels as TX<4> and RX<4> respectively. The repeater device 105 is now able to deal with native five-bit symbols across all of its interfaces. This allows the decode and encode stages at the receiving and transmitting port(s) to be eliminated, avoiding

the time required for these steps and hence reducing the delay through repeater 100.

Having an ability to reassign channel functions, either through hardware or software, provides additional pin savings while increasing flexibility and functionality of the repeater 100. It is possible to provide support for both TX and T4 protocols, on a per port or group of ports basis without adding pins by appropriately reconfiguring repeater devices 105 and interface device 110.

A TX protocol requires a false carrier (FLS_CRS) from a PHY device to the repeater device 105 while the T4 protocol does not use FLS_CRS. However, for the TX protocol, the COL channel can be denied by the repeater device 100, whereas for the T4 protocol the COL channel must be provided. To provide for flexible, per port/interface device TX/T4 support without adding dedicated channels is one feature of the preferred embodiment. The COL channel shown in FIG. 2 is made selectively configurable depending on which mode is desired. For use as a T4 PHY, the COL channel remains as described above. For TX PHY mode, repeater device 105 reconfigures the COL channel as the FLS_CRS channel. For TX operation, the TX PHY not only uses the COL channel as the FLS_CRS channel, it activates the CRS channel during only receive carrier, not for receive carrier or transmit carrier as defined in the 802.3u standard. A TX PHY indicates a collision condition to repeater device 105 by asserting CRS (receive active) and use of TX_EN (transmit active). Repeater device 105 detects the simultaneous transmit and receive activity, so it has no need of the COL channel when in TX PHY mode. Note that while Repeater Device 105 and Interface Device 110 can have their MIIs programmed to use the dedicated FLS_CRS pin when in the TX PHY mode, in addition, Interface Device 110 simultaneously provides an optional mechanism (as defined by IEEE Standard 802.3u) for indicating receive error across the MII. This is performed by asserting RX_ER, deasserting RX_DV, and sourcing the hexadecimal coded "E" (1110) representation onto the MII RXD<3:0> pins. While the transport of the coded value of false carrier is provided to

support repeater device implementations that do not have the dedicated FLS_CRS pin function, this comes at the expense of some decode delay in order to detect false carrier. The provision of the dedicated false carrier pin (per port) allows fast false carrier detect time at the expense of the additional pin complement. However, Interface Device 110 fully supports either option in the Repeater Device 105."

The COL channel remains in T4 mode without providing a FLS_CRS channel. Since T4 mode does not provide for a false carrier function, a T4 PHY device does not need a channel to signal false carrier information to the repeater device 105. Thus, twelve pins are saved while providing the ability for repeater device 105 to be used with different modes of PHY devices. As long as the mode setting is performed for groups of PHY devices, or all PHY devices, or through software configuration commands, the pin savings are maintained.

US Patent 5,539,737, incorporated herein by reference, describes security and some of the concerns of eavesdropping in 10Mb/s Ethernet networks. This describes how a particular port or ports may be identified to have data disrupted or allow data to pass 'clear'. However, in implementations where the PHY is integrated, the disrupt control provided by the repeater is easily communicated to the PHY. With external PHY channels, a means is needed to allow the disrupt function to be communicated without use of additional interface pins between the repeater device 105 and interface device 110. The preferred embodiment implements eavesdrop security for repeater 100 without adding additional dedicated channels between the repeater device 105 and each PHY device. The IEEE 802.3u standard provides a symbol, the 'HALT' symbol that in certain applications may seem to be an effective solution to eavesdrop protection. A PHY device responds to concurrent assertion of TX_EN and TX_ER by issuing the 'HALT' symbol. Unfortunately, concurrent assertion of TX_EN and TX_ER also indicates a transmit error which may not be appropriate to use in every situation that eavesdrop security is desired.

It is important therefore to differentiate between a normal transmit error code condition (sending the 'HALT' symbol), and the eavesdrop protection mode wherein an alternate symbol should be selected for transmission. A simple way to communicate this information between the repeater device 105 and any particular PHY device is through a special combination of the TX_EN and TX_ER channels of the MII as shown in TABLE II below.

TABLE II

TX_EN	TX_ER	INDICATION
0	0	Normal Inter-frame
0	1	Eavesdrop protection mode - Issue fixed symbol scrambling.
1	0	Normal Data Transmit, TXD<3:0> transmitted
1	1	Transmit error code, HALT transmitted

In the preferred embodiment, a PHY device may transmit a fixed symbol when the PHY device observes the eavesdrop protection encoding on its MII (the shared TX_ER channel and the dedicated TX_EN channel). The fixed mode would be selected to take into account issues such as backward compatibility with the existing implementations or effects such as crosstalk and/or EMI. Once determined, the eavesdrop protection code could be fixed for these devices. Alternatively, PHY devices may incorporate an MII register which would allow the programming of the symbol sent during eavesdrop protection. The default value of this register would be either the preferred value (as determined above) or could be set to any arbitrary symbol, including the 'HALT' symbol if desired. It would be the contents of this register that any particular PHY device would transmit upon observing the eavesdrop protection code.

In the preferred embodiment, each TX PHY device includes an independently selectable integrated carrier integrity machine (CIM). A TX PHY device is not normally expected to include a CIM, therefore the preferred embodiment desirably enables/disables the CIM function for each PHY device to allow the integrated device 110 to interoperate with

existing repeater devices available on the market other than the integrated repeater device 105, as well as with future more integrated devices (and devices more closely partitioned to the IEEE 802.3u standard).

Some existing integrated repeater devices that a user may desire to use in conjunction with the integrated interface devices 110 do not incorporate a carrier integrity monitor (CIM) state machine which is required by the current IEEE 802.3u standard. The carrier integrity monitor is similar to a link pulse or 'heartbeat' signal used in some Ethernet implementations. Thus, it is desirable to implement a CIM in the integrated interface device 110 so that together the devices (repeater device and interface devices) properly implement the CIM of the IEEE standard. In the preferred embodiment, it is desirable to provide one CIM for each PHY device of the interface device 110. The DISENDEC channel controls operation of all the CIMs in interface device 110.

When a CIM is turned on, or is not disabled, it monitors the carrier received from the Physical Medium Dependent layer (PMD) of the port and is responsible for generating FORCE_JAM and ISOLATE primitives as appropriate, according to the IEEE 802.3u specification. Whenever ISOLATE is true, the transmitting and receiving of the port is inhibited (the port is isolated similar to partition in the 10BASE-T specification). The isolated port will not respond to any transmit request received on the MII. The CIM of the isolated port ensures that the interface device 110 continues to issue IDLE symbols on the serial output of the isolated port regardless of the status of the associated TX_EN channel. Any activity received from the PMD of the port will not cause the assertion of the CRS, RX_DV, or RX_ER for that port. However, it will continue monitoring the activity on the medium.

The FORCE_JAM primitive of the CIM, when true, forces repeater device 105 to send JAM to all of its ports. Because an interface device 110 does not have control of all potential ports of repeater 100, an additional process is necessary to accomplish the task of causing all ports to

recognize the JAM, and to facilitate the propagation of the JAM process across all of the interface devices 110, a particular PHY device associated with a port for which the FORCE_JAM primitive is true asserts the CRS channel and maintains it asserted for as long as the FORCE_JAM primitive is true. Additionally, this PHY device transmits alternating "3" and "4" on the RXD channels. Note that an alternating "3" and "4" sequence is the JAM pattern for existing implementations of repeater circuits which translated into 4B/5B coded serial signal is a 010101... bit stream. This bit stream is also transmitted to the physical medium of the port by the PHY device.

If one port goes into the FALSE CARRIER state of the CIM state machine (FORCE_JAM is true) and there is no activity detected on any other port, repeater device 105 repeats the alternating "3" and "4" JAM pattern on the RXD channels to the other ports except to the port having the FALSE CARRIER. Thus, all ports send out the JAM pattern on their physical medium, since the port that detected FALSE CARRIER independently sources the JAM sequence.

If two ports are colliding and either one, or both, of the ports is in the FALSE CARRIER state, the 100RIC should send JAM to all the ports as in the normal collision case. In the case of the "ONE PORT LEFT" condition, if the false carrier ends last, all ports continue to transmit JAM until the end of the false carrier event described in the preceding scenario. However, if the false carrier event ends first, this port will switch from independently generating the JAM sequence to retransmitting the JAM sequence from the MII, and the JAM sequence does not end during the switch process. It is desirable, depending upon specific implementations, to minimize a time difference between a start of JAM on the port having the false carrier and the start of the JAM sequence on the other ports.

The integrated interface device 110, in the preferred embodiment shown in Fig. 2, is designed for repeater applications. The internal semiconductor device of integrated interface device 110 may also be repackaged for a switch

application. Fig. 3 is a schematic plan view of an alternate pin out option of an integrated switch interface device 300 using the same internal semiconductor device packaged for the integrated interface device 110 shown in Fig. 2.

The switch interface device 300 of Fig. 3 includes a 160 pin PQFP while the interface device 110 includes a 100 pin PQFP. Since a repeater application is typically much more price sensitive, the additional pin count reduction for interface device 110 is important.

As explained above, in the repeater application, a single RXD<3:0> and TXD<3:0> set of channels (pins), eight total, are multiplexed on the interface device 110 for all four ports of the PHY, with a combination of shared and dedicated control channels for the four ports. This multiplexing permits considerable pin savings over the full MII complement. Since the repeater receives from a single port at any given time, and transmits the same data on one or more of its ports, separation of TXD and RXD is necessary, but individual TXD and RXD nibble groups for each port are not necessary, since the data output from all transmitting ports is the same.

In a switch application, transmit data from any input data port is routed independently to one or more output ports, but not generally to all output ports. In addition, a switch allows many independent conversations to occur simultaneously, and may also permit full duplex operation, requiring each port to send and receive potentially different data at the same time. For the switch application, one full MII is provided for each port, with each MII having an independent TXD and RXD nibble complement.

There is a steering mode for the switch device that uses less than all of the MIIs. In this steering mode, only two of the four MIIs are active, and each one of the four PMD ports is independently coupled to either one of the MIIs. This permits 'load balancing' or 'port mobility' functions to be achieved.

Fig. 4 is a schematic diagram of a dual repeater 400 including a first repeater device 405, a second repeater

device 410, a network device 415 to interconnect the first repeater device 405 with the second repeater device 410, two switches 420 and two switch interface devices 300 (first switch interface device 300 and second switch interface device 300). Network device 415 is, in the preferred embodiment, a bridge or router which is known, and can be used for speed matching. Switch 420 independently routes signals from its four PMDs to either one of its 2 MIIs. Each MII of switch 420 is dedicated to one of the repeater devices, with corresponding outputs of the switches 420 coupled together for coupling to the appropriate repeater device. For example, the first MII output of each switch 420 is coupled to first repeater 405 and the second MII of each switch 420 is coupled to second repeater 410. Switch 420 includes four channels, one coupled to each MII output of switch interfaces 300. In the preferred embodiment, the switch 420 and Switch Interface Device 300 are integrated into the functionality of previously described Interface Device 110 (Figs. 1 and 2). In addition, the pin savings identified for the MII when operating in this "dual MII to quad PMD mode" can still be realized, again minimizing the pin requirements of first and second repeater device (405 and 410 respectfully). However, some additional pins may be necessary for clocking and or speed selection.

In operation, any MII output from a PHY device of first switch interface 300_1 may be routed to either first repeater device 405 or second repeater device 410. Similarly, any MII output from a PHY device of second switch interface device 300_2 may be routed to either first repeater device 405 or second repeater device 410. If both the first and the second repeater device operate at 100Mb/s, there would effectively be two collision domains, each operating at 100Mb/s. This provides for load balancing and an ability to move a port to a desired repeater domain.

A more preferred embodiment provides for first repeater device 405 to operate at 100Mb/s and for second repeater device 410 to operate at 10Mb/s. Thus, each MII from switches 420 to the repeater devices operate at different speeds. This is a valid use of the MII, which operates at 25

MHz (x4bits) for 100Mb/s operation and at 2.5 MHz (x4 bits) for 10Mb/sec operation. Each PHY device of the switch interface devices 300 are dual speed (10/100 capable) and designed to Auto-Negotiate between these two speeds. Such dual speed PHY devices, and Auto-Negotiation, are common and widely known in 10/100BASE-T implementations. By providing the dual MII for four PHY device ports, a 10/100 repeater is constructed, where PHY devices are either forced or allowed to steer themselves (after Auto-Negotiation has completed the speed negotiation of the link and corresponding end station of any particular port). In this way, each front panel port of repeater 400 can support either a 10Mb/s or a 100Mb/s station. When connected to the repeater port, the speed capability of the connected device is detected and the PHY device is coupled into the appropriate speed collision domain of the dual speed collision domain repeater.

In conclusion, the present invention provides a simple, efficient solution to a problem of providing a repeater including an integrated repeater device coupled to one or more integrated interface devices in a cost effective and flexible manner. While the above is a complete description of the preferred embodiments of the invention, various alternatives, modifications, and equivalents may be used. Therefore, the above description should not be taken as limiting the scope of the invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. An integrated device for use with a repeater front-end, the device comprising:

a first PHY having first receive channels for receiving data from the repeater, first transmit channels for transmitting data to the repeater and first control channels for transmitting and receiving control signals from the repeater front-end; and

a second PHY having second receive channels coupled to said first receive channels for receiving data from the repeater, second transmit channels coupled to said first transmit channels for transmitting data to the repeater, and second control channels independent from said first control channels for receiving and transmitting control signals from the repeater front-end.

2. An integrated device for use with a repeater front-end, the device comprising:

a first PHY and a second PHY, each PHY having a media independent interface operable in a first and a second mode, wherein said first mode includes a plurality of transmit channels for transmitting data to a repeater, a plurality of transmit channels for receiving data from said repeater, a transmit error channel for receiving a transmit error signal from the repeater, and a receive error channel for transmitting a receive error signal to the repeater, and wherein said second mode configures said transmit error channel as an additional transmit channel of said plurality of transmit channel and configures said receive error channel as an additional receive channel of said plurality of receive channels; and

a mode controller, coupled to said interfaces, for independently selecting one of said first and second modes for each said PHY.

3. A PHY comprising:

a media independent interface operable in a first and a second mode, wherein said first mode includes a plurality of transmit channels for transmitting data to a repeater, a plurality of transmit channels for receiving data from said repeater, a transmit error channel for receiving a transmit error signal from the repeater, and a receive error channel for transmitting a receive error signal to the repeater, and wherein said second mode configures said transmit error channel as an additional transmit channel of said plurality of transmit channels and configures said receive error channel as an additional receive error channel of said plurality of receive channels; and

a mode controller, coupled to said interface, for selecting one of said first and second modes.

4. An integrated device for use with a first repeater and a second repeater, said device comprising:

a first PHY having first data channels for receiving data from the first repeater, first transmit channels for transmitting data to the first repeater, first control channels for transmitting and receiving control signals from the repeater, and first input channels for receiving data signals to be transmitted to the first repeater;

a second PHY having second receive channels for receiving data from the second repeater, second transmit channels for transmitting data to the second repeater, second control channels for transmitting and receiving control signals from the second repeater, and second input channels for receiving data signals to be transmitted to the second repeater; and

a switch having a plurality of input channels for receiving data signals, and a plurality of output channels for transmitting data received on said plurality of input channels to one of said first and second PHYs.

5. The integrated device of claim 4, wherein the first repeater operates at a first speed and the second

repeater operates at a second speed different from said first speed.

6. The integrated device of claim 5, wherein said first speed is 10Mb/s and said second speed is 100Mb/s.

7. A PHY comprising:

a media independent interface operable in a first and a second mode, wherein said first mode includes a plurality of input channels for receiving data to be transmitted to a repeater, a carrier sense channel for transmitting a carrier sense signal to the repeater when the input channels are active, a transmit enable channel for receiving a transmit enable signal from the repeater, and a collision channel for transmitting a collision detected signal to the repeater, and wherein said second mode configures said collision channel as a false carrier channel for transmitting a false carrier signal to the repeater; and

a mode controller, coupled to said interface, for selecting one of said first and second modes.

8. A security device for use with a repeater, said device comprising:

at least one PHY having

a transmit enable channel for receiving a transmit enable signal from said repeater;

a transmit error channel for receiving a transmit error signal from said repeater; and

output channels for outputting a predetermined security symbol in response to a security signal asserted from the repeater on said enable and error channels.

9. The security device of claim 8, wherein said security signal is asserted when said enable signal is deasserted and said error signal is asserted.

10. A method of providing security in a PHY device having communication channels established between the PHY device and a repeater, comprising the steps of:

determining whether to apply a security signal to the PHY;

applying the security signal over the communication channels to the PHY; and

responding to the applied security signal to output a security symbol.

11. The method of claim 10 wherein said signal applying step further comprises the steps of:

asserting one of the communication channels which is recognized as a transmit error channel; and

deasserting one of the communication channels which is recognized as a transmit enable channel.

12. The method of claim 10 wherein said responding step further comprises the step of:

responding to the applied security signal to output a predetermined security symbol.

13. The method of claim 10 wherein said responding step further comprises the steps of:

generating programmably a security symbol; and

outputting said programmably generated security symbol.

14. A PHY device comprising:

transmit channels for transmitting data to a repeater;

receive channels for receiving data from said repeater;

control channels for transmitting and receiving control signals from said repeater;

input channels for receiving data to be transmitted to said repeater;

output channels for transmitting data received from said repeater; and

a carrier integrity monitor for monitoring the activity on said input channels.

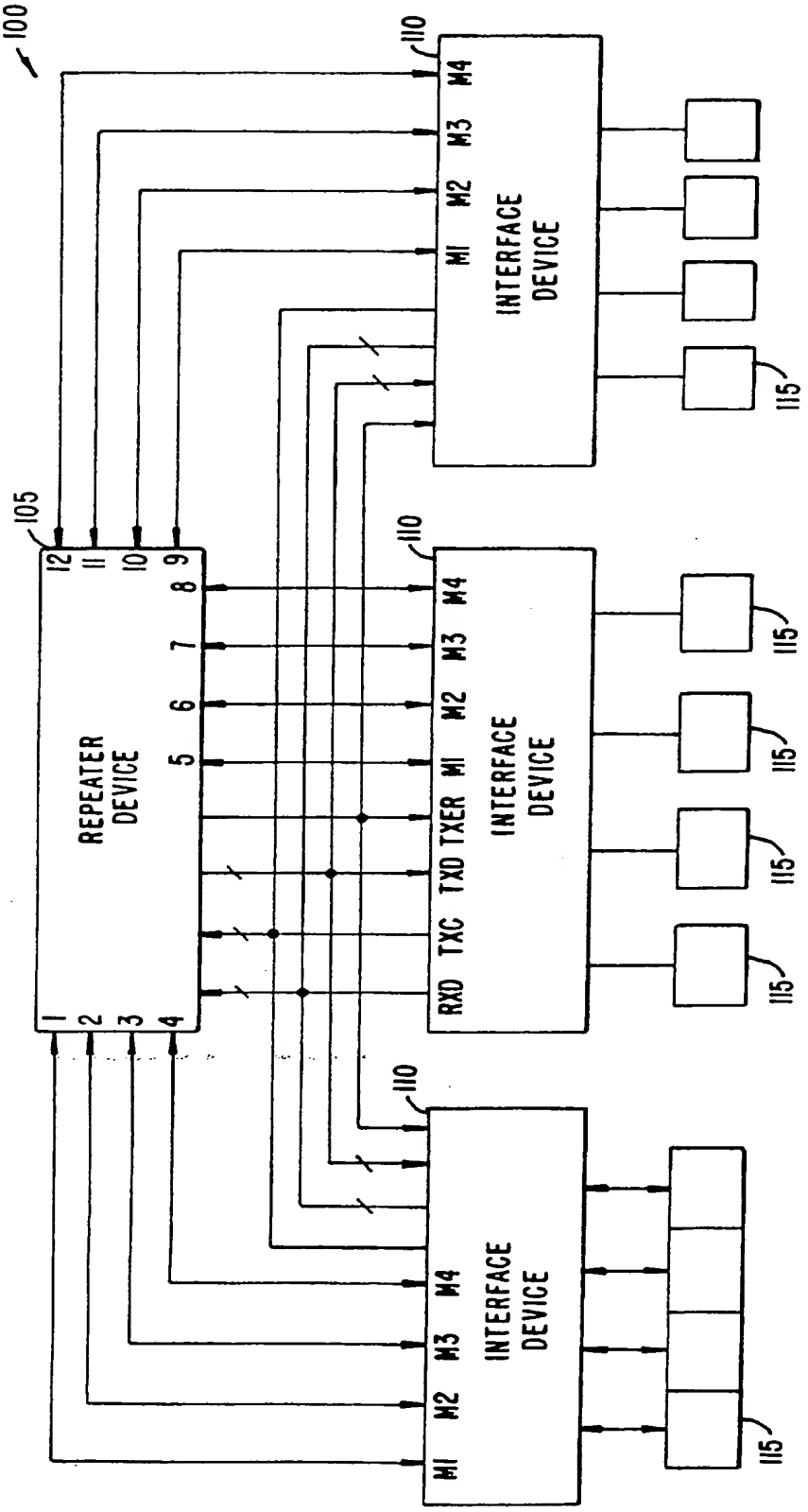
100
105
REPEATER DEVICE
12
11
10
9
8
7
6
5
1
2
3
4
110
INTERFACE DEVICE
M1
M2
M3
M4
RXD
TXC
TXD
TXER
115

FIG. 1.

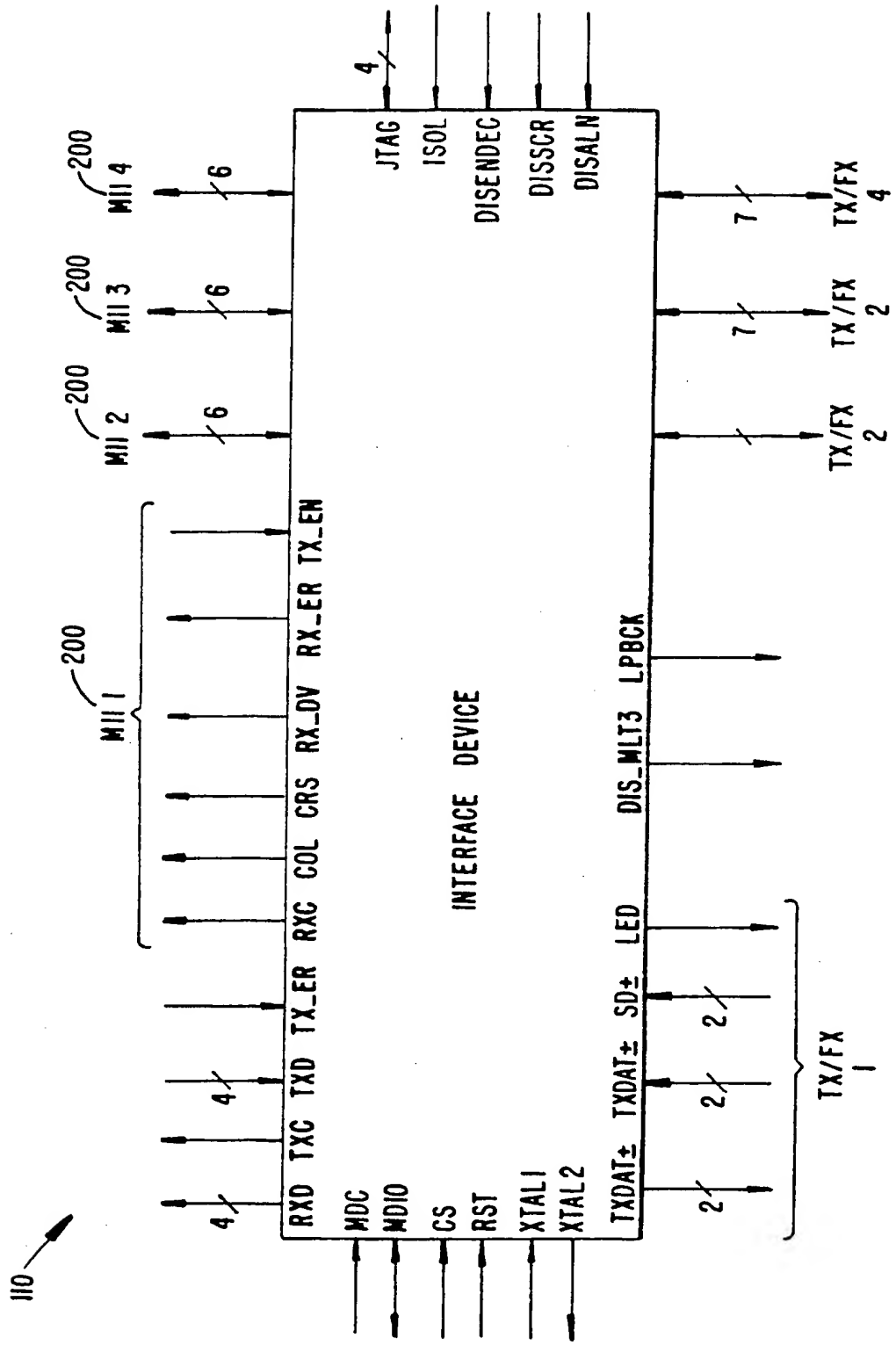
110
INTERFACE DEVICE
MII 1
200
MII 2
200
MII 3
200
MII 4
200
RXD
TXC
TXD
TX_ER
RXC
COL
CRS
RX_DV
RX_ER
TX_EN
MDC
MDIO
CS
RST
XTAL1
XTAL2
TXDAT±
TXDAT±
SD±
LED
DIS_MLT3
LPBCK
JTAG
ISOL
DISENDEC
DISSCR
DISALN
TX/FX 1
TX/FX 2
TX/FX 2
TX/FX 4

FIG. 2.

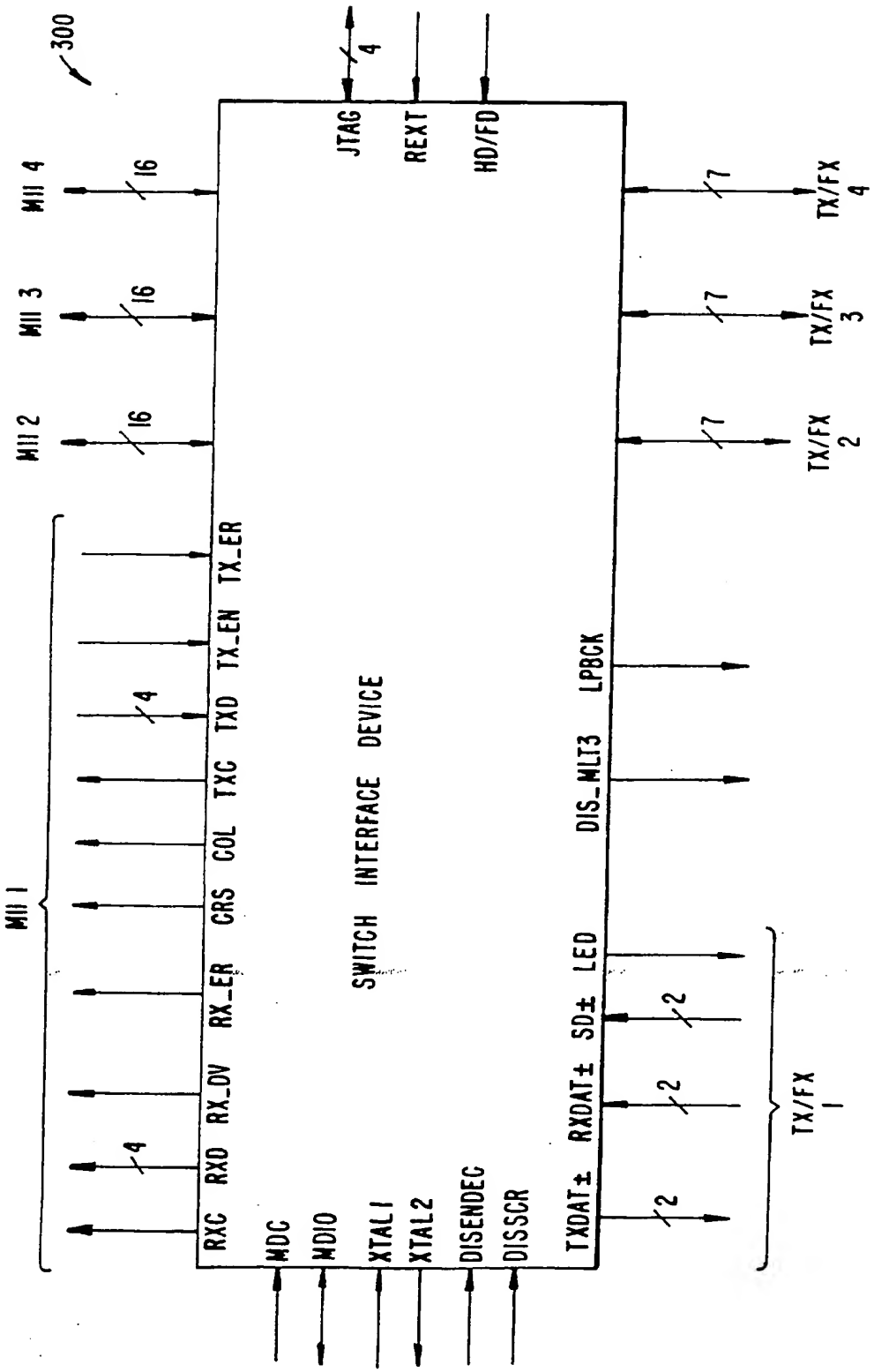
300
SWITCH INTERFACE DEVICE
JTAG
REXT
HD/FD
MII 4
MII 3
MII 2
MII 1
TX/FX 4
TX/FX 3
TX/FX 2
TX/FX 1
RXC
RXD
RX_DV
RX_ER
CRS
COL
TXC
TXD
TX_EN
TX_ER
MDC
MDIO
XTAL1
XTAL2
DISENDEC
DISSCR
TXDAT±
RXDAT±
SD±
LED
DIS_MLT3
LPBCK

FIG. 3.

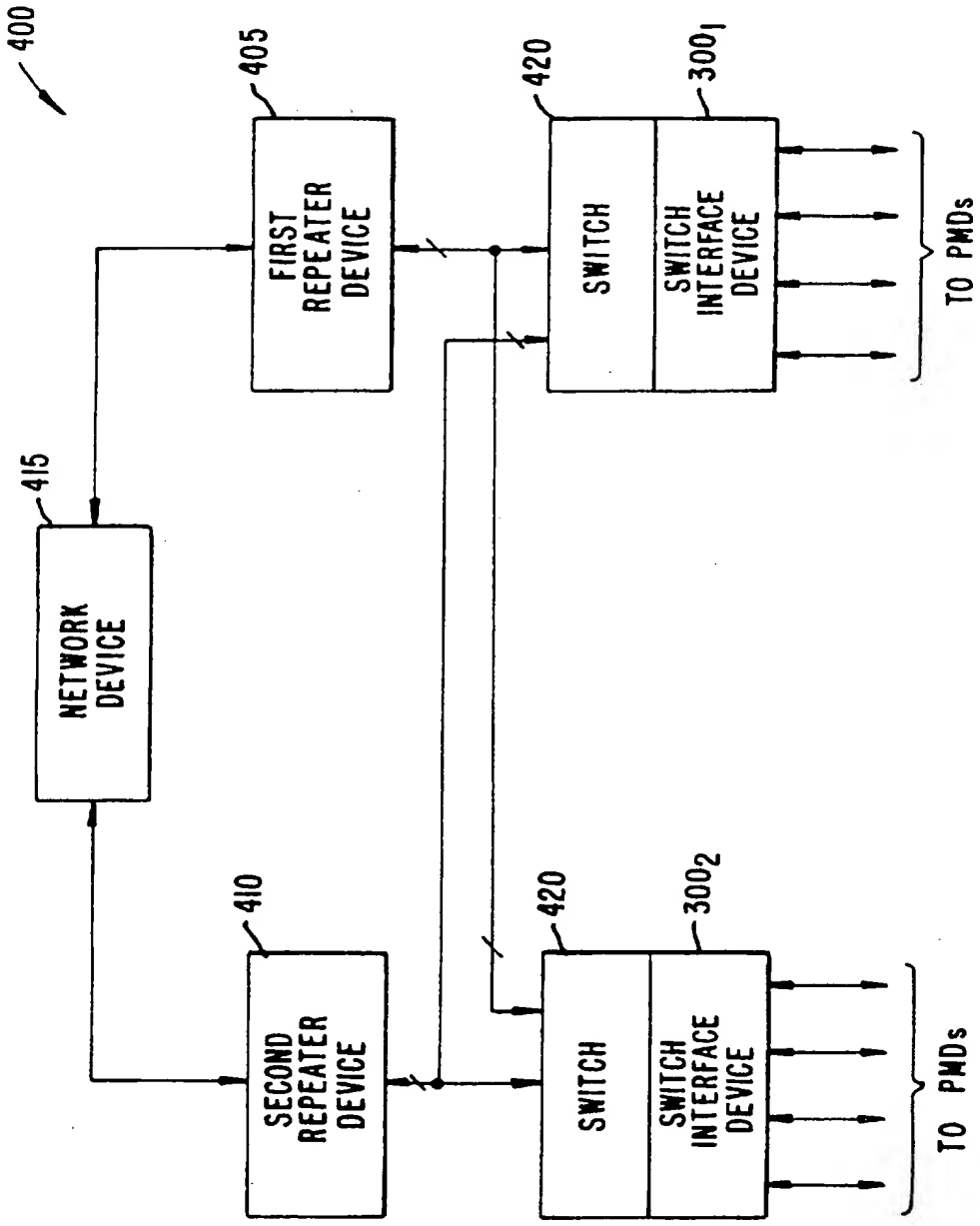

FIG. 4.

INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 97/03538

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L12/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ELECTRONIC ENGINEERING, vol. 67, no. 820, 1 April 1995, page 25/26, 28, 30 XP000501192 SOMER G: "ETHERNET TRANSCEIVER OFFERS UPGRADE FROM EXISTING NETWORKS" see page 25, left-hand column, line 1 - middle column, line 6 see page 26, right-hand column, line 2 - line 28 see page 28, left-hand column, line 55 - page 30, right-hand column, line 14 see figures 1,3,4	10
Y		12-14
A		1-4,6-11

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

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Date of the actual completion of the international search	Date of mailing of the international search report
18 June 1997	01. 07. 97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Vaskimo, K

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 431 751 A (BICC PUBLIC LIMITED COMPANY) 12 June 1991 see column 1, line 1 - line 22 see column 1, line 54 - column 2, line 16 see column 3, line 40 - column 4, line 2	12,13
A		1,2,4,5, 8,10,14

Y	EP 0 495 575 A (NATIONAL SEMOCONDUCTOR CORPORATION) 22 July 1992 see page 3, line 14 - line 52 see page 4, line 10 - line 22 see page 5, line 22 - line 24 see page 7, line 13 - line 47 see page 8, line 3 - line 8 see page 9, line 42 - line 46 see page 16, line 47 - page 18, line 25 see page 32, line 30 - page 33, line 25	14
A		1,2,4,5, 8,10,12, 13

A	ELECTRONIC DESIGN, vol. 43, no. 6, 20 March 1995, page 155/156, 158, 160 XP000509380 GOLDBERG L: "100BASE-T4 TRANSCEIVER SIMPLIFIES ADAPTER, REPEATER, AND SWITCH DESIGNS" see page 155, line 1 - line 34 see page 158, middle column, line 13 - page 160, left-hand column, line 34	1-4,6-8, 10,14

A	ELECTRONIC DESIGN, vol. 42, no. 1, 10 January 1994, page 45/46, 48, 50, 55/56 XP000424509 BURSKY D: "CHIP SET DELIVERS 100 MBITS/S TO THE DESKTOP" see page 46, middle column, line 12 - page 48, left-hand column, line 15 see figures 1,3	1-4,6-8, 10,14

A	EDN ELECTRICAL DESIGN NEWS, vol. 40, no. 24, 23 November 1995, pages 53-56, 58, 60, XP000546015 WRIGHT M: "NETWORK-SWITCH ICS SIMPLIFY DESIGN AND SLASH PER-PORT COSTS" see page 55, left-hand column, line 25 - right-hand column, line 26	1,2,4-6

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INTERNATIONAL SEARCH REPORT

Intl onal Application No
PCT/US 97/03538

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DATA COMMUNICATIONS, vol. 23, no. 12, 1 September 1994, page 49/50 XP000462381 SAUNDERS S: "SWITCH MIXES UNLIKE LANS AT AN UNLIKELY LOW PRICE XYLAN'S OMNISWITCH IS THE ONLY SWITCH TO SUPPORT ETHERNET, TOKEN RING, FDDI, AND ATM NETWORKS IN ONE BOX" see the whole document ---	4-6
A	WESCON TECHNICAL PAPERS, vol. 35, 1 November 1991, pages 232-237, XP000320542 CRAYFORD I: "10BASE-T IN THE OFFICE" see page 232, right-hand column, line 1 - page 234, left-hand column, line 30 ---	8,10,14
A	IEEE COMMUNICATIONS MAGAZINE, vol. 34, no. 8, August 1996, pages 64-73, XP000616890 MOLLE M ET AL: "100BASE-T / IEEE 802.12/PACKET SWITCHING" see page 66, right-hand column, line 27 - page 67, right-hand column, line 31 -----	

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INTERNATIONAL SEARCH REPORT

information on patent family members

Int onal Application No
PCT/US 97/03538

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 431751 A	12-06-91	AT 118142 T	15-02-95
		CA 2029577 A	07-06-91
		DE 69016618 D	16-03-95
		DE 69016618 T	17-08-95
		ES 2071785 T	01-07-95
		JP 3190446 A	20-08-91
		US 5386470 A	31-01-95
		US 5161192 A	03-11-92
EP 495575 A	22-07-92	JP 4335731 A	24-11-92
		US 5396495 A	07-03-95
		US 5384767 A	24-01-95
		US 5299195 A	29-03-94
		US 5293375 A	08-03-94
		US 5430726 A	04-07-95